CLAIMS

What is claimed is:

1. A method for forming a interconnect opening comprising:

providing a semiconductor structure having a first dielectric layer and a lower interconnect;

forming a passivation layer over said first dielectric layer and said interconnect;

forming a stack dielectric layer over said passivation layer;

patterning and etching said stack dielectric layer to form an upper interconnect opening;

forming an interface layer over the passivation layer, on sidewalls said upper interconnect opening and on top of said stack dielectric layer;

removing said interface layer from the stack dielectric but not from the sidewalls of said upper interconnect opening:

etching the passivation layer and interface layer to open the bottom of the upper interconnect opening.

2. A method for forming a interconnect opening comprising:

providing a semiconductor structure having a first dielectric layer and a lower interconnect;

forming a passivation layer over said first dielectric layer and said interconnect;

forming a stack dielectric layer over said passivation layer;

patterning and etching said stack dielectric layer to form an upper interconnect opening;

etching of said passivation layer to open a bottom of the upper interconnect opening;

forming an interface layer over the lower interconnect, on sidewalls of said upper interconnect opening and on top of said stack dielectric layer.

3. The method of claim 2 wherein said interface layer is removed from the stack dielectric, and from the lower interconnect, but not from the sidewalls of said upper interconnect opening.

4. The method of claim 1, wherein said stack dielectric layer consists of one dielectric layer.

5. The method of claim 1, wherein said stack dielectric layer is comprised of a second layer and a third dielectric layer.

6. The method of claim 1, wherein the method is for forming a dual damascene opening.

7. The method of claim 1, wherein a metal is deposited in the upper interconnect opening to form an upper interconnect.

8. The method of claim 5, wherein an etch stop layer is formed between the second and third dielectric layers.

9. The method of claim 1, wherein a cap layer is formed on the stack dielectric layers.

10. The method of claim 1, wherein the interface layer is a copper (I) compound or a copper (II) compound.

11. The method of claim 1, wherein the interface layer is a copper sulfide interface layer.

12. The method of claim 1, wherein the interface layer is deposited by using a chemical vapor deposition.

13. The method of claim 1 where said interface layer is formed by a reaction comprising: reacting [copper (Beta-diketonate)(L)] complex with a sulfide-containing compound.

14. The method of claim 13 wherein L in the [copper (Beta-diketonate)(L)] complex comprises one of the following: an alkene, an alkyne or a phosphine.

15. The method of claim 13 wherein the sulfidecontaining compound comprises either ammonium sulfide or hydrogen sulfide.

16. The method of claim 1, wherein the interface layer is removed partially by plasma-assisted dry etching wherein etching chemistry comprises one or more gases from a group containing hydrogen bromide, chlorine, ammonia, silicon tetrachloride, chlorine-substituted silane, nitrogen, argon and hydrogen.

17. The method of claim 1, wherein the lower interconnect is comprised of one or more conductors from a group containing copper, aluminum, aluminum alloy, tungsten, titanium, titanium nitride, tantalum, tantalum nitride and tungsten nitride.

18. The method of claim 1, wherein the lower interconnect is comprised of copper.

19. The method of claim 1, wherein the dielectric layers are one of the following:

a. non-porous undoped silicon oxide,
b. porous undoped silicon oxide
c. non-porous doped silicon oxide,
d. porous doped silicon oxide,
e. non-porous organic material, porous organic material,
f. non-porous doped organic materials,
g. porous doped organic material,
h. phosphosicate glass, or
i. SiO2.

20. The method of claim 1, wherein the passivation layer is one of the following;

a. silicon nitride,

b. silicon oxynitride,

c. silicon carbide, or

d. boron nitride.

21. An interconnect opening comprising:

A semiconductor structure having a first dielectric layer and a lower interconnect;

passivation layer over said first dielectric layer and said interconnect;

a stack dielectric layer over said passivation layer;

an upper interconnect opening through said stack dielectric layer and said passivation layer having sidewalls consisting of an interface layer comprised of copper sulfide.

22. The interconnect of claim 20, wherein said stack dielectric layer consists of one dielectric layer.

23. The interconnect of claim 20, wherein said stack dielectric layer is comprised of a second layer and a third dielectric layer.

24. The interconnect of claim 20, wherein a metal is in the upper interconnect opening to form an upper interconnect.

25. The interconnect of claim 22, wherein there is an etch stop layer between the second and third dielectric layers.

26. The interconnect of claim 20, wherein a cap layer is on the stack dielectric layers.

27. The interconnect of claim 20, wherein the lower interconnect is comprised of one or more conductors from a group containing copper, aluminum, aluminum alloy, tungsten, titanium, titanium nitride, tantalum, tantalum nitride and tungsten nitride.

28. The interconnect of claim 20, wherein the lower interconnect is copper.

29. The interconnect of claim 20, wherein the dielectric layers are one of the following:

a. non-porous undoped silicon oxide,

b. porous undoped silicon oxide

c. non-porous doped silicon oxide,

d. porous doped silicon oxide,

e. non-porous organic material, porous organic material,

f. non-porous doped organic material,

g. porous doped organic material,

h. phosphosicate glass, or

i. SiO2.

30. The interconnect of claim 20, wherein the passivation layer is one of the following:

a. silicon nitride,

b. silicon oxynitride,

c. silicon carbide, or

d. boron nitride.

31. A method for forming a interconnect opening comprising:

providing a semiconductor structure having a first dielectric layer and a lower interconnect;

forming a passivation layer over said first dielectric layer and said interconnect;

forming a stack dielectric layer over said passivation layer;

patterning and etching said stack dielectric layer to form an upper interconnect opening;

forming an interface layer over the passivation layer, on sidewalls said upper interconnect opening and on top of said stack dielectric layer wherein the interface layer is formed by a reaction comprising: reacting [copper (Beta-diketonate)(L)] complex with a sulfide-containing compound; wherein L in the [copper (Beta-diketonate)(L)] complex comprises one of the following: an alkene, an alkyne or a phosphine;

removing said interface layer from the stack dielectric but not from the sidewalls of said upper interconnect opening:

etching the passivation layer and interface layer to open the bottom of the upper interconnect opening.